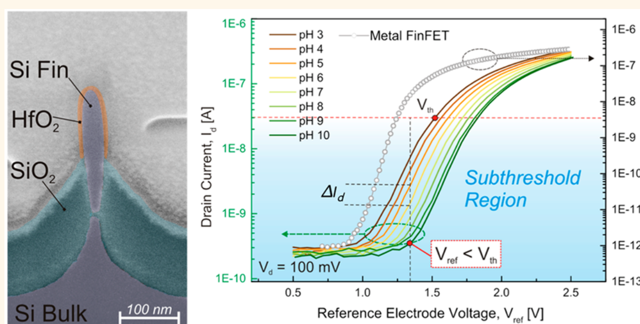
Sensing with Advanced Computing Technology: Fin Field-Effect Transistors with High-k Gate Stack on Bulk Silicon

Sara Rigante,[*,†] Paolo Scarbolo,[‡] Mathias Wipf,[§] Ralph L. Stoop,[§] Kristine Bedner,[||] Elizabeth Buitrago,[†] Antonios Bazigos,[†] Didier Bouvet,[†] Michel Calame,[§] Christian Schönenberger,[§] and Adrian M. Ionescu[†]

[†]Nanoelectronic Devices Laboratory, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland, [‡]Department of Electrical, Management and Mechanical Engineering, University of Udine, 33100 Udine, Italy, [§]Department of Physics, University of Basel, 4003 Basel, Switzerland, and [||]Laboratory for Micro- and Nanotechnology, Paul Scherrer Institut, 5232 Villigen, Switzerland

ABSTRACT Field-effect transistors (FETs) form an established technology for sensing applications. However, recent advancements and use of high-performance multigate metal—oxide semiconductor FETs (double-gate, FinFET, trigate, gate-all-around) in computing technology, instead of bulk MOSFETs, raise new opportunities and questions about the most suitable device architectures for sensing integrated circuits. In this work, we propose pH and ion sensors exploiting FinFETs fabricated on bulk silicon by a fully CMOS compatible approach, as an alternative to the widely investigated silicon nanowires on silicon-on-insulator substrates. We also provide an analytical insight of the concept of sensitivity for the electronic integration of sensors. N-channel fully depleted FinFETs with critical dimensions on the order of 20 nm and HfO_2 as a high-k gate insulator have been developed and characterized, showing excellent electrical properties, subthreshold swing, SS $\sim$ 70 mV/dec, and on-to-off current ratio, $I_{on}/I_{off} \sim 10^6$, at room temperature. The same FinFET architecture is validated as a highly sensitive, stable, and reproducible pH sensor. An intrinsic sensitivity close to the Nernst limit, $S = 57$ mV/pH, is achieved. The pH response in terms of output current reaches $S_{out} = 60\%$. Long-term measurements have been performed over 4.5 days with a resulting drift in time $\delta V_{th}/\delta t = 0.10$ mV/h. Finally, we show the capability to reproduce experimental data with an extended three-dimensional commercial finite element analysis simulator, in both dry and wet environments, which is useful for future advanced sensor design and optimization.



KEYWORDS: Fin field-effect transistor sensor · FinFET · ISFET · pH sensing · high-k dielectric · low power · sensing integrated circuits · long-term stability

The first pioneering works implementing micro- and nanotechnologies for chemical and biological sensing applications date back more than 40 years.[1] In the past decade, they have become the center of attention of the research and the industry domains, following the urge to develop portable and zero-power healthcare devices.

Despite the fact that microcantilevers[2,3] and mass spectroscopy[4,5] are two of the most sensitive label-free techniques, they both require the use of complex instrumentation to acquire and process signals. In contrast, field-effect transistor (FET) sensors are highly oriented toward smart sensing because of their cheap manufacturing cost, mechanical resistance, and reliability over time. In order to achieve circuit integration and large-scale production, a FET sensor should fulfill the constraints of a good sensor as much as the ones of a good electronic device. A FinFET is a vertical transistor with lateral conductive channels, as shown in Figure 1. The gate (whether metallic or through a liquid) generates an electrostatic potential surrounding the device almost in its totality, providing an excellent channel control. In terms of performance, this results in a steeper subthreshold slope upon scaling, that is, higher readout sensitivity. Due to a precise assessment of the technological development, a FinFET also provides high stability and repeatability. The FinFET

* Address correspondence to sara.rigante@epfl.ch.

Received for review November 10, 2014 and accepted March 27, 2015.

Published online March 27, 2015
10.1021/nn5064216

© 2015 American Chemical Society

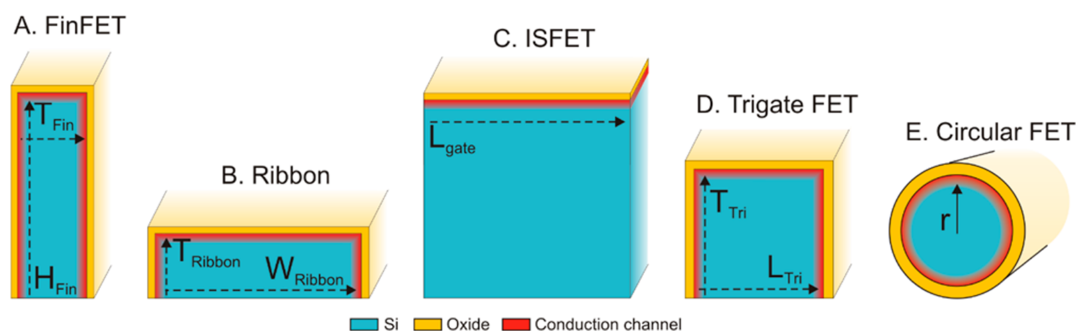


Figure 1. Cross sections of a FinFET (A) and of other SiNW architectures (B–E) commonly implemented in sensing-related works (Table 1).

TABLE 1. State-of-the-Art SiNWs for Sensing Applications: Technology

reference	technology
this work	TD, bulk Si, FinFET
microsens SA[8]	TD, bulk Si, ISFET
Abe *et al.*[9]	TD, bulk Si, ISFET
Lee *et al.*[10]	TD, SOI, ribbon FET
Park *et al.*[11]	TD, SOI, ribbon FET
Yoo *et al.*[12]	TD, SOI, ribbon FET
Kim *et al.*[13]	TD, SOI, trigate FET
Ahn *et al.*[14]	TD, SOI, trigate FET
Ahn *et al.*[7]	TD, bulk Si, buried FinFET
Vu *et al.*[15]	TD, SOI, ribbon FET
Cui *et al.*[16]	TD, SOI, ribbon FET
Tarasov *et al.*[17]	TD, SOI, ribbon FET
Chen *et al.*[18]	TD, SOI, ribbon FET
Zhang *et al.*[19]	TD, SOI, trigate FET
Li *et al.*[20]	TD, SOI, trigate FET
Hahm *et al.*[21]	BU, SOI, GAA
Stern *et al.*[22]	TD, SOI, ribbon FET
Zheng *et al.*[23]	TD, SOI, not available
Kim *et al.*[24]	TD, SOI, ribbon FET
Li *et al.*[25]	BU, SOI, GAA
Wang *et al.*[26]	BU, SOI, GAA
Zhang *et al.*[27]	TD, SOI, ribbon FET
Chiang *et al.*[28]	TD, SOI, ribbon FET
Patolsky *et al.*[29]	BU, SOI, GAA
Bae *et al.*[30]	TD, SOI, ribbon FET

advantages are well-known in electronics,[6] and 22 nm FinFETs are implemented today in Intel's latest microprocessor on bulk Si.

FinFET for Sensing Integrated Circuits. Table 1 shows relevant works related to silicon nanowires (SiNWs) for sensing applications focusing on three technological aspects: the fabrication approach (TD = top-down, BU = bottom-up), the substrate (bulk Si, silicon-on-insulator (SOI)), and the device architecture (GAA, trigate, *etc.*). Figure 1 shows the cross sections of the geometries that have been identified in the cited works:

(A) FinFET: with $H_{Fin}/T_{Fin} > 1$
(B) ribbon FET: with $W_{ribbon}/T_{ribbon} > 1$, including trapezoidal and triangular silicon nanowires
(C) ISFET: ion-sensitive field-effect transistor based on the standard metal–oxide semiconductor (MOSFET)
(D) trigate FET: with $W_{Tri}/T_{Tri} \approx 1$
(E) GAA FET: gate-all-around, circular wires.

While the majority of the devices found in literature have been fabricated using a top-down methodology, some are also based on silicon nanowires obtained by a bottom-up approach from molecular precursors, a method which is not yet compatible with complementary metal–oxide semiconductor (CMOS) integration. Almost the totality of the cited works are based on SiNWs fabricated on SOI substrates. Here, we seek to provide a reliable alternative on bulk Si in order to extend the compatibility of FET sensors to the CMOS industry. The device architecture is rarely addressed in literature. Most of the available works are based on devices with rather large width, and vertical transistors are not yet available. The work of Ahn *et al.*[7] presents a device that shares the most similarities with the FinFET presented here. However, only the top-side of the vertical FET has been exploited as a sensing surface, while the body is embedded and controlled by lateral gates for amplification. On the other hand, in order to fully exploit the capabilities of the FinFET, we have completely immersed the body in solution to be controlled by a uniform potential applied through a reference electrode.

Readout Sensitivity: Ideality and Limits of FET Devices. The MOSFET and the ISFET share a physical limit, which is usually derived from the Boltzmann statistics, used as approximation of the Fermi–Dirac statistics in the classical regime. Indeed, the fundamentals of this classical limit can be traced back to a former concept, the Gibbs free energy[31] that combines the enthalpy and entropy of a closed system in a single value.

For a bulk MOSFET, the subthreshold slope (SS) is the variation of the drain current, I_d, according to gate potential, V_g, in the subthreshold region:[32]

$$\mathrm{SS} = \frac{\delta V_g}{\delta(\log I_d)} = \frac{\delta V_g}{\delta \Phi_S} \cdot \frac{\delta \Phi_S}{\delta(\log I_d)} = \left(\frac{kT}{q}\ln(10)\right) \cdot \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) = n \cdot m \quad (1)$$

with Φ_S being the surface potential at the silicon–oxide interface, k the Boltzmann constant, T the

temperature, C_D and C_{it} are the capacitances associated with the depletion region (in the semiconductor) and the interface trap states (at the semiconductor–insulator interface), respectively, and C_{ox} the gate oxide capacitance. The first term of eq 1, also known as n-factor, represents the physical limit previously mentioned, and it is equal to ~59 mV/dec at room temperature (T = 300 K). The second term, also known as body m-factor, describes the coupling between the gate potential and the surface potential. For an ideal FET device, m = 1, meaning that any variation of V_g is perfectly coupled to the surface potential Φ_S, giving rise to an equal increase in the subthreshold regime.

For the ISFET, the variation of the potential at the liquid–insulator interface, $\Delta\Psi$, is similarly coupled to the variation of potential of the bulk solution, for example, the pH change in the bulk solution ΔpH_B:[33]

$$|\Delta\Psi(\mathrm{pH})| = \left(\frac{kT}{q}\ln(10)\right)\cdot\left(\frac{\beta}{\beta+1}\right)\cdot\Delta\mathrm{pH_B} = n\cdot\alpha \quad (2)$$

where β symbolizes the buffer capacitance of the sensing surface and ΔpH_B = 1. Equation 2 is usually referred to as the Nernst equation or Nernst limit. The potential difference arises from the oxide surface reactions necessary to reach the electrochemical equilibrium. According to the density of the amphoteric sites, specific for each oxide, the factor α will approach the unit and $\Delta\Psi$ will reach the maximum value of 59 mV/pH. Similarly to the MOSFET, only an ideal coupling between the solution and the oxide surface allows the maximum change in the solution to be fully transduced to the device. The potential variation $\Delta\Psi$ is commonly read in terms of the FET threshold voltage variation ΔV_{th}. Such variation represents the intrinsic sensitivity of the sensor, and it does only depend on the surface oxide and the chemical species' properties. The device geometry and its electronic parameters do not interfere with ΔV_{th}. Alternatively, the sensing variation can be acquired through I_d at fixed V_{ref}. In this case, the two physical limits of the MOSFET and the ISFET can be merged together into a common parameter describing, at the same time, the quality of the surface transduction and the electronic readout capability of the FET device. This parameter is specifically defined here as readout sensitivity S_{out} equal to the relative drain current variation before and after a change in the solution, and it can be developed as follows:

$$S_{out} = \frac{\delta I_d}{I_d} = \frac{\delta I_d}{\delta V_g}\cdot\frac{\delta V_g}{I_d} = \frac{\delta I_d}{I_d\cdot\delta V_g}\cdot\delta V_g$$
$$= \frac{\delta\ln(I_d)}{\delta V_g}\cdot\delta V_g = \frac{\delta V_g}{\mathrm{SS}} = \frac{\Delta V_{th}}{\mathrm{SS}} = \frac{\alpha}{m} \quad (3)$$

Remembering that $0 \leq \Delta V_{th} \leq 59$ mV/pH, while 59 mV/dec $\leq$ SS $< \infty$:

- for an ideal FET sensor, S_{out} = 1
- for a surface oxide featuring at least full coupling with ΔpH_B, $0 \leq S_{out} \leq 1$
- for a FET device featuring at least the ideal SS, $0 \leq S_{out} \leq 1$

S_{out} can univocally represent the quality factor of a FET sensor when looking at electronic integration, and it depends on the device architecture. Moreover, S_{out} can be written as

$$S_{out} = \frac{\Delta V_{th}}{\mathrm{SS}} = \frac{g_m}{I_d}\cdot\Delta V_{th}\cdot\ln(10) \quad (4)$$

where g_m/I_d is the transconductance-to-current ratio, which is used in analog IC design.[34]

RESULTS AND DISCUSSION

HfO_2 for Reliable and Integrable Sensors. Hafnium dioxide has been chosen as the gate oxide for both liquid and metal gate FinFET. HfO_2 satisfies all the criteria of the semiconductor CMOS industry, and it is proven to provide a pH response close to the Nernst limit. Though no mathematical correlation has yet been determined between the dielectric constant and the oxide pH response, it is known that SiO_2, Si_3N_4, Al_2O_3, and HfO_2 provide an increasing pH response[9,35,36] and they feature, with the same order, a higher dielectric constant. A reasonable explanation is the high level of ionicity, I_b, that high-k dielectrics feature.[37] Such parameter is, in turn, connected to the coordination number which expresses how many oxygen neighbors a central atom (Si, Hf) has. A higher coordination number in the bulk will result in a higher density of hydroxyl groups at the surface and, as a consequence, higher pH sensitivity. Moreover, upon certain conditions of the electrolyte, an oxide expressing the Nernstian sensitivity is not sensitive to salt concentration,[17] ensuring high linearity from one pH value to another. The use of HfO_2 is therefore an indispensable technology choice.

One of the main difficulties while depositing HfO_2 onto a Si surface is the control of the interface layer (IL) between HfO_2 and Si. It is possible to observe such phenomenon in the transmission electron microscope (TEM) image of a Si–HfO_2–Al stack in Figure 2. Many works refer to this IL as a silicide, namely, $Hf_xSi_{1-x}O_y$.[38] The presence of this interface layer inevitably causes hysteresis, due to a negative charge trapping/detrapping mechanism at the oxide–substrate boundary. Despite the fact that many works related to SiNWs for sensing applications have made use of high-k dielectrics, the subject of hysteresis is rarely addressed. Indeed, it represents a true obstacle for reliable sensors.

We have investigated several technological factors and their impact on the HfO_2 performance in terms of hysteresis ΔV_H, dielectric constant ε_{HfO_2}, and breakdown voltage V_{BD}. We have first compared three

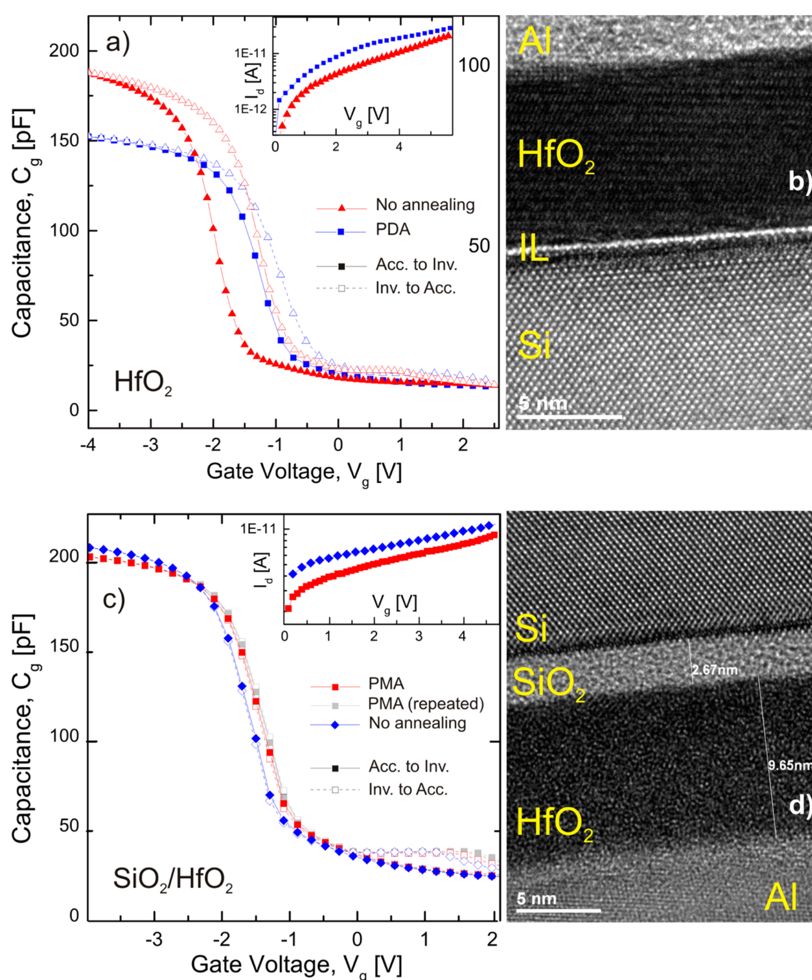


Figure 2. *C*−*V* and leakage current (inset) measurements for the (a) Si−HfO_2−Al and (c) Si−SiO_2−HfO_2−Al sensing gate stack. TEM images of the (b) Si−HfO_2−Al stack with uncontrolled IL and (d) Si−SiO_2−HfO_2−Al with no IL.

samples treated with standard RCA cleaning before the atomic layer deposition (ALD) of a 10 nm thick HfO_2 layer. One sample was then treated with an annealing performed at 500 °C for 1 h in a N_2 environment (postdeposition annealing, PDA). As reported in Table 2, the annealing reduces the hysteresis from 0.72 to 0.41 V by lowering the trap density at the interface, but it also decreases the dielectric constant from 18 to 14 and the breakdown voltage from 12.5 to 10.5 V. Comparison of the TEM image on the left with the one on the right shows that this is due to the crystallization of HfO_2. On the other hand, if the annealing is performed in the presence of a uniform metal layer (postmetallization annealing, PMA), no effects are reported. The second impact factor is an additional cleaning procedure after the standard RCA. Piranha (a mixture of H_2SO_4 and H_2O_2) and a HF-last (hydrofluoric) steps have been tested. The RCA followed by the Piranha in combination with a PDA achieved a quite good result in terms of hysteresis with $\Delta V_H = 0.18$ V. The dielectric constant is $\varepsilon_{HfO_2} = 15$. This value is the lowest hysteresis value that was possible to achieve by depositing only HfO_2. On the contrary, the HF-last results in a significant hysteresis and quite low V_{BD}. In agreement with the presented results, Green *et al.*[39] have reported the use of a chemical oxide (the oxide produced by a Piranha cleaning) as IL results in almost no barrier to film nucleation and the most two-dimensionally continuous HfO_2 film. All values have been extracted from the *C*−*V* measurements presented in Figure 2.

TABLE 2. Electrical Properties of HfO_2 Treated with Different Fabrication Procedures

oxide	RCA	annealing	ΔV_H	ε_{HfO_2}	V_{BD}
HfO_2	standard	no	0.72 V	18	12.4 V
HfO_2	standard	PDA	0.41 V	14	10.5 V
HfO_2	standard	PMA	0.69 V	18	13.7 V
HfO_2	Piranha	PDA	0.18 V	15	12.7 V
HfO_2	HF-last	PDA	0.8 V	15	9.1 V
SiO_2/HfO_2	standard	no	**8 mV**	**17**	**16.5 V**

From the insets of Figure 2a,c, it is also possible to observe the leakage current through the oxide, which does not exceed 10 pA up to 5 V for any of the conditions tested.

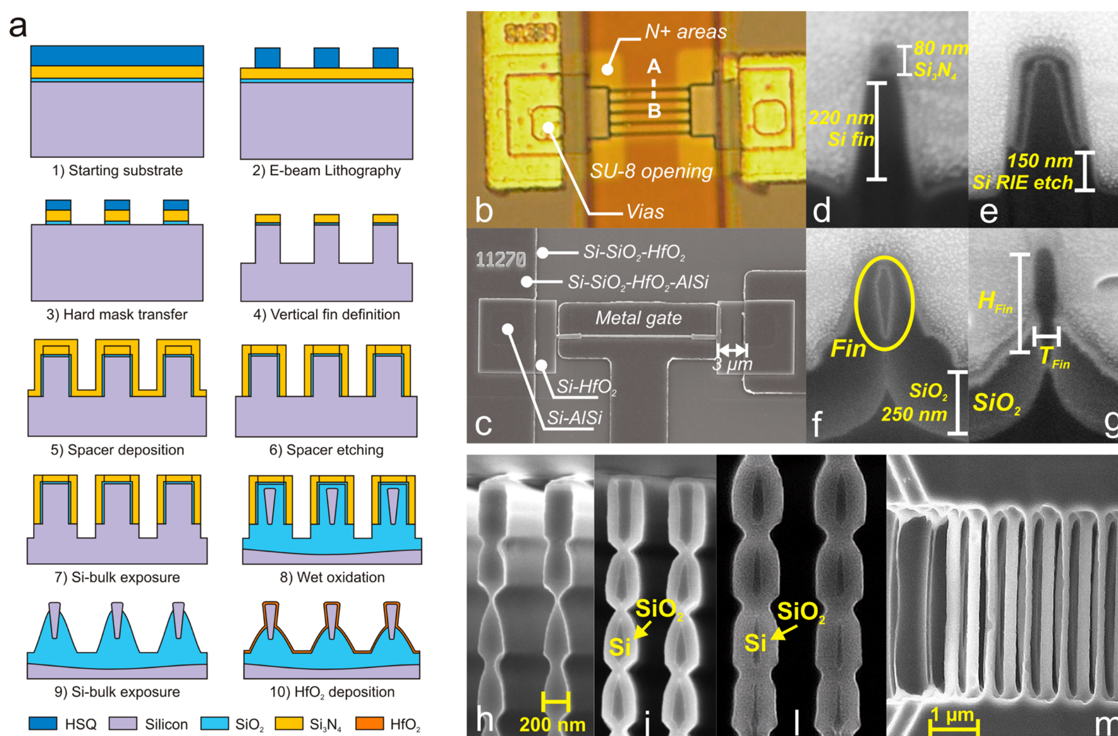


Figure 3. (a) Simplified process flow for two-dimensional FinFETs. (b) Optical top image of a FinFET array for sensing applications with SU-8 next to the FET channels. (c) SEM top image of a single FinFET with a metal gate. (d) SEM cross sections obtained by focused ion beam during the fabrication process: definition of the vertical Si fin with top Si_3N_4 hard mask. (e) Deposition of the Si_3N_4 spacers. (f) Si fin after wet oxidation and growth of a 250 nm thick SiO_2 layer. (g) Si fin after Si_3N_4/SiO_2 etching and exposure of the fin surface. (h) Here we show a version of our process that can provide 3D fins formed with a combination of anisotropic and isotropic etches *before* oxidation to vertically stack multiple fin channels. (i) Nonsharp scallop 3D fins after oxidation. (l) Sharp scallop with O_2 step included after oxidation and (m) top side of 3D fin channel view after Buffered Oxide Etching (BOE) release. Note that the electrical and sensing characteristics reported in this work correspond to devices in panels b−g.

The complete suppression of the hysteresis is achieved by the thermal growth of 2.5 nm SiO_2 between the Si and HfO_2. As shown in Figure 2c, no hysteresis and repeatability are obtained for the SiO_2−HfO_2 stack. The obtained hysteresis is $\Delta V_H < 8$ mV for a V_g sweep between −4 and 4 V, fully covering the accumulation and the inversion regimes. From the TEM image of Figure 2d, it is clearly possible to observe that no IL is now present between any layers.

Stability and pH Response of the FinFET Sensors. The FinFETs were fabricated according to a top-down approach on a bulk silicon substrate. The fabrication aimed at a specific and reproducible geometry of the FinFETs, with the body of the devices isolated from the substrate similarly to what is expected on SOI wafers, and a high-k dielectric (HfO_2) has been used as the sensing gate oxide. The whole fabrication process can be simplified as shown in Figure 3a. A well-controlled wet oxidation of the etched silicon fins protected by the Si_3N_4 spacers is used to provide a local SOI structure for every Fin device. The final dimensions of the fabricated device are 16 nm $\leq T_{Fin} \leq$ 40 nm and 50 nm $< H_{Fin} <$ 120 nm, with H_{Fin}/T_{Fin} always greater than 3. The quality and uniformity of the FinFETs have been first tested on the metal gate devices. Subthreshold slope values are in the range of 70 mV/dec $\leq$ SS $\leq$ 81 mV/dec with the steepest value achieved for the smallest T_{Fin} = 16 nm. The device uniformity has been validated by measuring the SS of six devices at different wafer locations. The results are SS = 71 ± 1 mV for T_{Fin} = 16 nm, SS = 74 ± 1.5 mV for T_{Fin} = 20 nm, SS = 79 ± 2 mV for T_{Fin} = 30 nm, and SS = 81 ± 2 mV for T_{Fin} = 40 nm (see Supporting Information). As for the SS, we have extracted the V_{th} values of the corresponding devices, and the variation is in the range of 0.5 mV $\leq \Delta V_{th} \leq$ 50 mV. The ratio between ON and OFF currents is $10^5 \leq I_{on}/I_{off} \leq 10^6$, with the highest value $I_{on}/I_{off} = 2 \times 10^6$ obtained for T_{Fin} = 40 nm. Such excellent results imply that there is no parasitic leakage current through the bulk Si, and the local SOI on bulk offers equivalent performance to a fully depleted FinFET on SOI.

The FinFET sensors have been tested in liquid gate configuration, and long-term stability measurements have been performed over 4.5 days. The liquid environment has been kept at constant pH 6. Every 30 min, the pumping system was automatically activated to renew the liquid on top of the sensors. After a stabilization time of about 2 min, the V_{th} was extracted at I_{th} = 2 nA. The total observation time is 105 h, where the first 24 h have been deleted due to a pumping failure that occurred during the night, as it is possible to observe in Figure 4. All devices feature a HfO_2 oxide with a

thickness of t_{HfO_2} = 8 nm. The wafers have been treated with a full RCA cleaning followed by a Piranha step, thus the presence of a chemical oxide between Si and HfO_2 of around 1 nm is highly probable. Table 3 collects drift data related to sensing SiNWs with similar oxide thickness.

The long-term stability of the FinFETs was investigated over 4.5 days, and excellent results were achieved. Looking at Figure 4, the baseline drift in time is $\delta V_{th}/\delta t$ = 0.13 mV/pH for a single-wire FinFET with T_{Fin} = 30 nm (D1 and D2). The maximum spread of the V_{th} from the baseline is the standard error $SE_{V_{th}}$ = ±1 mV. In addition, by monitoring two identical entities located at different wafer positions, the two data sets superpose. The inset of Figure 4a shows the subtraction of the two populations of data with a residual ΔV_{th} = 0.6 mV. This result implies an excellent reproducibility of the devices at the wafer level, which

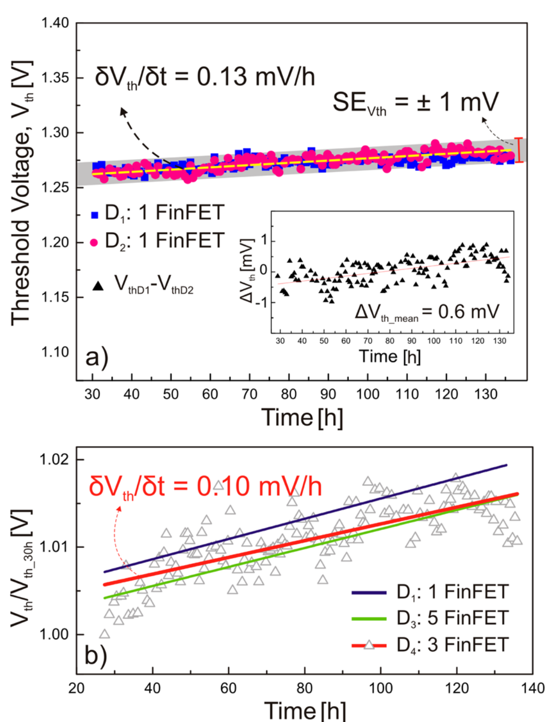


Figure 4. FinFET long-term stability measurement at constant pH 6. (a) V_{th} for equal single-wire FinFET sensors at different die locations, with the inset showing the two data set difference. (b) Drift in time for three different devices normalized at the initial V_{th} at time (h) = 30: D1 (single wire with T_{Fin} = 30 nm), D3 (three wire FinFET with T_{Fin} = 20 nm), and D4 (five wire FinFET with T_{Fin} = 30 nm).

has been achieved by a proper calibration of the fabrication on bulk Si. For nanoscale devices, in fact, geometrical differences, especially at the device corners, may cause significant V_{th} variations due to volume inversion for critical dimensions around 10 nm.[40] In Figure 4b, the baseline drift normalized with respect to V_{th0} for two other devices is also reported. For a three-wire FinFET (D3) with T_{Fin} = 20 nm, the drift is 0.10 mV/h, while for a five-wire FinFET with T_{Fin} = 30 nm, it is 0.12 mV/h. Overall, these results firmly prove the stability of the presented devices. More statistics are necessary to comment on the effect of number or size of the devices. In comparison to related works, our drift time is highly improved, as shown in Table 3. The main cause of drift is usually related to the quality of the outer layer in terms of ion diffusion through the sensing oxide itself, a phenomenon that increases with time due to the hydration of the first oxide layers in contact with the solution.[41] However, the FinFET architecture may also be claimed to be a better structure for highly reliable and stable devices and sensors in time.[42]

The pH response of the latest optimized pH sensing FinFETs is presented together with the stability results. The devices achieved an almost full Nernstian response with ΔV_{th} = 57 mV/pH between pH 3 and pH 10, as shown in Figure 5a for the HfO_2 layer. As expected, for a SiO_2 sensing oxide, the response is much lower, ΔV_{th} = 30 mV/pH. The sensitivity is also influenced by the salt concentration, and the pH response is not linear in the considered pH range. Moreover, the HfO_2 FinFET exhibits excellent output sensitivity, as defined in eq 1. The drain current I_d has been monitored in time, exchanging solution at different pH values from pH 10 to pH 3 and backward, as reported in Figure 5b. The FinFET has been biased at V_{ref} = 1.5 V, V_{ds} = 100 mV at pH 10. According to the I_d (V_{ref}) characteristics, such bias corresponds to the subthreshold region of the FinFET where the subthreshold slope is steep and constant. As a consequence, S_{out} reaches its maximum values, 50% ≤ S_{out} ≤ 60%, between pH 10 and pH 5. The highest absolute current variations, ΔI_d = 105 nA/pH, are instead achieved when the characteristic is shifted toward the linear region, for 3 ≤ pH ≤ 5. From Figure 5b, it is also possible to observe the reversibility of the current level for the same pH values. By calculating the mean I_d value for each population of data at a specific pH value, the current hysteresis can be

TABLE 3. Comparison of Stability and pH Response with SiNW-Related Works[a]

	this work	30	9	14	43	8
$\delta V_{th}/\delta t$	0.1 mV/h or 0.07%	1.88 mV/h (HfO_2)	0.3 mV/h (Al_2O_3)	27 mV/pH (SiO_2)	0.24%	0.2 mV/pH
$S = \Delta V_{th}$	57 mV/pH (HfO_2)	55.3 mV/pH (HfO_2)	58 mV/pH (Al_2O_3)	22 mV/pH (SiO_2)		53.7 mV/pH (Al_2O_3)
S_{out}	0.4 dec/pH or 60%/pH		≈0.15 dec/pH		10.85%/pH	
ΔI_d	105 nA/pH	10.80 nA/pH				

[a] All data are reported as maximum values; some data have been converted from the original work for comparison purposes.

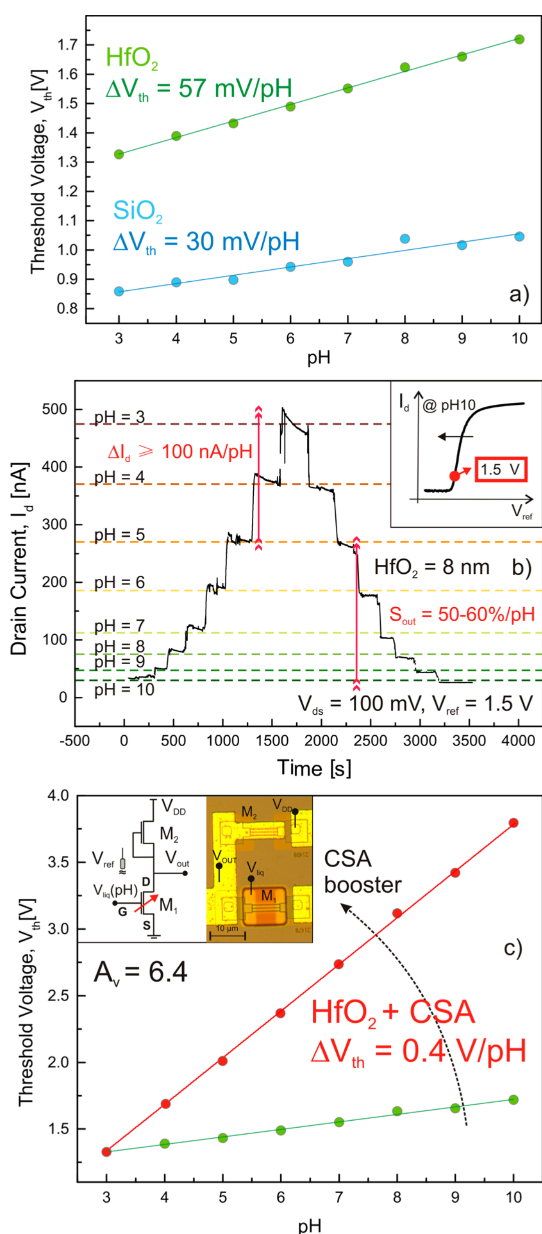


Figure 5. (a) V_{th} (pH) for a single FinFET with T_{Fin} = 30 nm for a HfO_2 and SiO_2 gate oxide. (b) Drain current I_d for a FinFET sensor during a time period of 1 h from pH 10 to pH 3 and backward at V_{ref} = 1.5 V and V_{ds} = 100 mV. (c) Amplification gain obtained by a two-component common source amplifier.

estimated. The higher current hysteresis is ΔI_H = 8.6 nA at pH 7, and overall, the average current hysteresis is ΔI_H = 5.6 nA. As we have demonstrated in the previous section, the hysteresis can be completely suppressed by the thermal growth of a thin SiO_2 layer prior to the ALD.

For comparison purposes, we have reported S_{out} in Table 3, but we have mentioned how these sensitivities depend on the biasing point and the operating region. The expression described in eq 1 given in dec/pH could be used as standard figure of merit to describe both sensing oxide and device performances. In the presented work, with ΔV_{th} = 57 mV/pH and the liquid gate SS = 150 mV/dec, S_{out} = 0.4 dec/pH. The SS of the liquid-gated FinFETs turned out to be less than the one obtained for the metal gate FinFET for which S_{out} would reach 0.8 dec/pH. This phenomenon is probably due to different interface traps and charges for the Si–oxide–metal stack with respect to the Si–oxide–liquid one, and it would need further studies. Another possible cause of this degradation is the presence of leakage current and consequence drop of the channel potential, but this has not been observed for our devices.

In Figure 5c, we propose the amplification of the sensing signal, obtained by a two-component common source amplifier (CSA) that we previously presented.[44] Anyway, in the previous work, the readout was limited by the use of defective HfO_2 which did not reach a full pH response. Here, the final output response reaches ΔV_{th} = 0.4 V/pH due to the combination of a high-quality HfO_2 and the CSA architecture with gain A_v = 6.4. It is important to notice that such a readout unit has been fabricated *in situ* with the same fabrication process used for single FinFETs. This proves the implementation of the same FET architecture for both sensing and circuit units.

Moreover, the dissipated power is limited in the range from tens to hundreds of nanowatts, that is, 8 nW ≤ P_{Fin} ≤ 150 nW for V_{ds} = 100 mV, according to the operating regime. The other applied voltages are 0.5 V ≤ V_{ref} ≤ 2.5 V and V_b = 0 V at the backgate. The applied voltage at the backgate is, indeed, very important to guarantee the compatibility of the sensor with CMOS ICs. Only in ref 13 is the power consumption clearly reported, with 3 nW ≤ P ≤ 15 nW for $I_d \leq 10^{-7}$ A, in agreement with our results.

Technology Computer-Aided Design Simulations toward More Complex ICs. Three-dimensional finite element analysis (FEA) simulations of the FinFET device (Sentaurus Device I-2013.12) were performed and compared to the experimental data. Figure 6 shows the comparison between measurements and simulations in dry (Figure 6a) and wet environments (Figure 6b). In the former case, the silicon channel is controlled by capacitive coupling through a metal gate deposited by Al sputtering, while, in the latter case, the metal gate is replaced by an electrolyte solution biased with a flow through a Ag/AgCl reference electrode, often called the liquid gate. To simulate the wet environment, an extension and more accurate version of the technology computer-aided design (TCAD) model presented in ref 45 was used. The electrolyte solution is described as a zero band gap semiconductor material. As demonstrated in ref 45, electron and hole intrinsic concentrations (N_C, N_V) have been modified in order to have the right molar concentration and charge neutrality in the bulk. The chemical species of the electrolyte can be

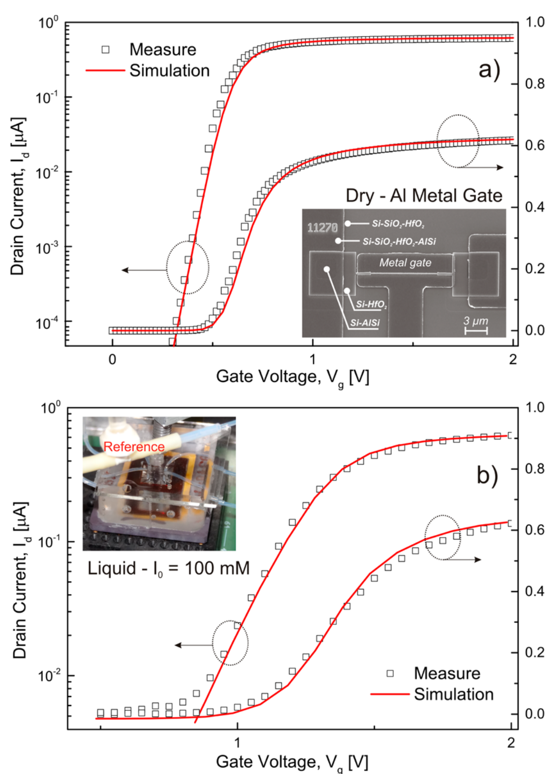


Figure 6. Measured and simulated $I_d(V_g)$ for a (a) metal and (b) liquid (bottom) gate FinFET (top) with logarithmic (left axis) and linear (right axis) scale.

simulated by modifying their mobility, in agreement with the electrolyte ions, and also, the medium dielectric constant is modified accordingly. Moreover, since the electrolyte ions cannot approach the surface arbitrarily closed, the hafnium gate oxide has been covered by a thin dielectric layer with 20 μF/cm^2 capacitance in order to replicate the Stern layer.[35] The ionic strength of the solution I_0 has been set to I_0 = 100 mM.

From the comparison of the metal and liquid gate FinFET characteristics, it is evident that the subthreshold slope is different between dry and wet conditions. The most probable origin of this phenomenon is the sensing surface modification, which occurs by charge trapping/detrapping at the interface states and ion penetration through the gate oxide. This interpretation has been confirmed and replicated by the TCAD simulations introducing traps at the channel/gate—-oxide interface. Acceptor traps from the midgap to the conduction band, and donor traps from the midgap to the valence band, both with a uniform distribution. In dry environment simulations, the trap concentration was 2×10^{12} cm^{-2} eV^{-1}, while in the wet case, a concentration of 2×10^{13} cm^{-2} eV^{-1} was used. All the other parameters, such as the doping concentrations and the device dimensions, have been kept at the nominal values in both dry and wet environments, and they correspond to the ones mentioned in the previous sections.

CONCLUSIONS

The main advantages of a FinFET as sensing element have been identified to be sensitivity, low power operation, stability, and reliability. In terms of sensitivity, excellent results have been obtained. However, for a given FET device with a specific intrinsic sensitivity and subthreshold slope, similar results can be achieved with other multigate devices or planar MOSFETs. The FinFETs reported in this work have been realized by a top-down approach on bulk Si by a controllable and scalable process flow, providing a valuable alternative to SOI substrates, commonly used for SiNW sensors.

The use of bulk Si with respect to SOI does not have any influence on the sensing properties or on the electrostatic control. Note that the use of the backgate for sensing SiNWs on SOI is not compatible with CMOS monolithic integration.

We have implemented the same FinFET architecture as both sensing and logic devices (in stand-alone and inverter configurations) with excellent electrical characteristics. The FinFET structure has been optimized to behave as an electronic switch with excellent electrostatic control, that is, SS = 70 mV/dec and $I_{on}/I_{off} = 10^6$, and sensing properties, such as S_{out} = 60% and $\Delta I_d = 10^2$ nA/pH. A HfO_2 gate oxide has been implemented for supporting a full pH response with ΔV_{th} = 57 mV/pH. The reliability of the oxide in terms of minimizing the electrical hysteresis has been addressed, proposing a controlled interfacial layer for sensing applications which achieved $\Delta V_H \leq 8$ mV. The drift in time has been measured to be $\delta V_{th}/\delta t$ = 0.1 mV/pH. Metal- and liquid-gated FinFETs have been implemented together into a two-component circuit unit, providing an amplified V_{th} shift of ΔV_{th} = 0.4 V/pH.

The combination of the stability and pH response results proves that, in the case of our FinFET sensor, there is no further trade-off between sensitivity and stability[43] nor a need for a thick oxide layer.[46]

Jointly optimizing the electronic and sensing properties has resulted in pH sensors with state-of-the-art features: (i) full and constant pH response, (ii) high readout sensitivity and high current variation, (iii) robust signal-to-noise ratio, (iv) low power consumption and voltage supply, (v) enhanced long-term stability and repeatability.

The experimental measurements have been accurately matched with FEA simulations in both dry and wet environments. The possibility to simulate the liquid environment represents an important achievement for the design of reliable sensing circuits.

The reported sensing platform based on highly stable, low-power FinFETs on bulk Si can be used for efficient label-free sensing for noninvasive simultaneous monitoring of human physiological signals, in terms of pH and other chemical and biological entities.

In conclusion, FinFETs are demonstrated to be high-profile candidates for integrated biosensing electronic

systems. The use of scalable high-k dielectric FinFETs for both sensing and circuit applications is, in fact, in accordance with the material and physics constraints which coincide with Moore's law of scaling, and it is fully compatible with CMOS integration, paving the way toward sensing integrated circuits.

METHODS

Technology. Two-dimensional arrays of FinFETs on bulk Si have been fabricated by a unique step of e-beam lithography (EBL), followed by four photolithography steps. The limited use of EBL makes it highly reproducible and apt to parallel batch production. The calibration and the validation of the geometrical and process oxidation parameters have been determined by FEA simulations.[47] The starting substrate is a p-type silicon wafer with doping concentration $N_D \approx 5 \times 10^{16}$ cm^{-3}. The EBL step is realized by exposure of hydrogen silsequioxane resist (HSQ), deposited on a Si_3N_4/SiO_2 hard mask (Figure 3a, 1). The patterned HSQ (Figure 3a, 2) is then transferred into the Si_3N_4 mask by SF_6-based deep reactive ion etching (RIE, Figure 3a, 3) and into the silicon substrate (200 nm) by Cl_2-based RIE (Figure 3, 4). The so-called Si_3N_4 spacers are formed by low-pressure chemical vapor deposition of a 50 nm thick Si_3N_4 layer (Figure 3a, 5) and Si_3N_4/Si etching (Figure 3a, 6 and 7). For the bulk Si insulation, 300 nm of SiO_2 is grown by wet oxidation, detaching and isolating the vertical fins from the bulk (Figure 3a, 8). Source and drain pads are implanted with phosphorus at 25 keV for a resulting concentration of N_A= 10^{20} cm^{-3}. The fin surface is then exposed by dip hydrofluoric acid (Figure 3a, 9) and covered by 8 nm of HfO_2 deposited by ALD (Figure 3a, 10). Figure 3 shows a sequence of SEM images of the FinFET cross sections, obtained by focused ion beam, from the vertical fin definition to the surface exposure. The electrical connections of the devices are made by $AlSi_{1\%}$ lines patterned by lift-off and vias of $3 \times 3\,\mu m^2$ that are etched by Ar ion milling through the HfO_2. For the FinFETs implemented as circuit units, an $AlSi_{1\%}$ metal gate was also deposited. After validation of the process by electrical characterization, SU-8 openings were patterned next to the FET sensing channels to prevent the contact between liquid and the metal connections, as shown in Figure 3b. Finally, the wafer was diced, and each die was glued into a chip carrier and connected by Au wires to a chip carrier.

FinFETs can also be fabricated in 3D arrays by an alternative process. In this configuration, the microcavity in which the FinFETs are allocated can act as a trapping site for proteins or other biological species, as it is possible to observe in Figure 3h−m. Different methods are available to produce 3D FinFET arrays.[48] They all have in common the deposition of a low-temperature oxide mask, which is patterned by an EBL/RIE step. In order to fabricate <150 nm fins smaller than 150 nm and create straight walls, a combination of anisotropic SF_6 and C_4F_8 dry etchings is used, as an alternative to the common BOSCH process. Then, isotropic SF_6 etching is used to separate one Fin from the other. With this method, only the top fin has straight side walls as a consecutive formation of droplet-shaped fins is promoted instead (Figure 3h). In a variation of this process route, an O_2 step was introduced after the C_4F_8 passivation and before the SF_6 isotropic etch to produce rounder separations, straighter walls (Figure 3i) and to reduce the droplet-shape appearance of the Fins.

TCAD Simulations. Simulations have been performed with a general purpose TCAD (Synopsys Sentaurus Device I-2013.12) which is based on FEA and offers simulation capabilities in a broad range of categories including semiconductor devices.

In order to simulate the electrolyte solution, a new material has been defined in the TCAD environment based on the idea that carriers in semiconductors and ions in solutions can be described with similar equations, based on the Boltzmann statistics. It is thus possible, using the functionalities of Sentaurus TCAD, to define a 1:1 electrolyte material with all the characteristics of a semiconductor except: (i) a zero band gap, (ii) a constant permittivity ($\sim 80\varepsilon_0$), (iii) appropriate mobility values[49] (depending on which ions are simulated), and (iv) a density of states for electrons (anions) an holes (cations) such that $N_C = N_V = N_A I_0 10^{-3}$ cm^{-3}, where N_A is Avogadro's number and I_0 is the ion molar concentration, in order to satisfy the charge neutrality. Finally, to avoid unphysical results, it is necessary to disable the temperature dependency of the model parameters whenever the temperature is different from the model reference value.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This project has been funded by the Swiss national program Nano-Tera within the project "NanowireSensor" (ref. 611_61). We would like to thank Prof. L. Selmi from University of Udine for the fruitful discussions and constant support.

Supporting Information Available: In the supporting information we provide data about FinFET uniformity. Experimental Subthreshold Slope values of FinFET with metal gates are provided according to different thicknesses and different wafer locations. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Bergveld, P. Thirty Years of ISFETOLOGY: What Happened in the Past 30 Years and What May Happen in the Next 30 Years. *Sens. Actuators, B* **2003**, *88*, 1–20.
2. Zhang, J.; Lang, H.; Huber, F.; Bietsch, A.; Grange, W.; Certa, U.; McKendry, R.; Güntherodt, H.-J.; Hegner, M.; Gerber, C. Rapid and Label-Free Nanomechanical Detection of Biomarker Transcripts in Human RNA. *Nat. Nanotechnol.* **2006**, *1*, 214–220.
3. Burg, T. P.; Godin, M.; Knudsen, S. M.; Shen, W.; Carlson, G.; Foster, J. S.; Babcock, K.; Manalis, S. R. Weighing of Biomolecules, Single Cells and Single Nanoparticles in Fluid. *Nature* **2007**, *446*, 1066–1069.
4. Russell, S. C.; Czerwieniec, G.; Lebrilla, C.; Steele, P.; Riot, V.; Coffee, K.; Frank, M.; Gard, E. E. Achieving High Detection Sensitivity (14 zmol) of Biomolecular Ions in Bioaerosol Mass Spectrometry. *Anal. Chem.* **2005**, *77*, 4734–4741.
5. Song, P.; Hershey, N. D.; Mabrouk, O. S.; Slaney, T. R.; Kennedy, R. T. Mass Spectrometry Sensor for *in Vivo* Acetylcholine Monitoring. *Anal. Chem.* **2012**, *84*, 4659–4664.
6. Colinge, J. P. *FinFETs and Other Multi-Gate Transistors*; Springer: Berlin, 2008.
7. Ahn, J.-H.; Kim, J.-Y.; Choi, K.; Moon, D.-I.; Kim, C.-H.; Seol, M.-L.; Park, T. J.; Lee, S. Y.; Choi, Y.-K. Nanowire FET Biosensors on a Bulk Silicon Substrate. *IEEE Trans. Electron Devices* **2012**, *59*, 2243–2249.
8. Microsens. Ion Sensitive Field Effect Transistor—ISFET. Available at http://www.microsens.ch/products/chemical.htm.
9. Abe, H.; Esashi, M.; Matsuo, T. ISFET's Using Inorganic Gate Thin Films. *IEEE Trans. Electron Devices* **1979**, *26*, 1939–1944.
10. Lee, J.; Lee, J.-M.; Lee, J. H.; Lee, W. H.; Uhm, M.; Park, B.-G.; Kim, D. M.; Jeong, Y.-J.; Kim, D. H. Complementary Silicon Nanowire Hydrogen Ion Sensor with High Sensitivity and Voltage Output. *IEEE Electron Device Lett.* **2012**, *33*, 1768–1770.
11. Park, I.; Li, Z.; Pisano, A. P.; Williams, R. S. Top-Down Fabricated Silicon Nanowire Sensors for Real-Time Chemical Detection. *Nanotechnology* **2010**, *21*, 015501.
12. Yoo, S. K.; Yang, S.; Lee, J.-H. Hydrogen Ion Sensing Using Schottky Contacted Silicon Nanowire FETs. *IEEE Trans. Nanotechnol.* **2008**, *7*, 745–748.

13. Kim, S.; Rim, T.; Kim, K.; Lee, U.; Baek, E.; Lee, H.; Baek, C.-K.; Meyyappan, M.; Deen, M. J.; Lee, J.-S. Silicon Nanowire Ion Sensitive Field Effect Transistor with Integrated Ag/AgCl Electrode: pH Sensing and Noise Characteristics. *Analyst* **2011**, *136*, 5012–5016.
14. Ahn, J.-H.; Kim, J.-Y.; Seol, M.-L.; Baek, D. J.; Guo, Z.; Kim, C.-H.; Choi, S.-J.; Choi, Y.-K. A pH Sensor with a Double-Gate Silicon Nanowire Field-Effect Transistor. *Appl. Phys. Lett.* **2013**, *102*, 083701.
15. Vu, X. T.; Eschermann, J. F.; Stockmann, R.; Ghosh-Moulick, R.; Offenhausser, A.; Ingebrandt, S. Top-Down Processed Silicon Nanowire Transistor Arrays for Biosensing. *Phys. Status Solidi A* **2009**, *206*, 426–434.
16. Cui, Y.; Wei, Q.; Park, H.; Lieber, C. M. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science* **2001**, *293*, 1289–1292.
17. Tarasov, A.; Wipf, M.; Stoop, R. L.; Bedner, K.; Fu, W.; Guzenko, V. A.; Knopfmacher, O.; Calame, M.; Schönenberger, C. Understanding the Electrolyte Background for Biochemical Sensing with Ion-Sensitive Field-Effect Transistors. *ACS Nano* **2012**, *6*, 9291–9298.
18. Chen, Y.; Wang, X.; Erramilli, S.; Mohanty, P.; Kalinowski, A. Silicon-Based Nanoelectronics Field-Effect pH Sensor with Local Gate Control. *Appl. Phys. Lett.* **2006**, *89*, 223512.
19. Zhang, G.-J.; Chua, J. H.; Chee, R.-E.; Agarwal, A.; Wong, S. M.; Buddharaju, K. D.; Balasubramanian, N. Highly Sensitive Measurements of PNA−DNA Hybridization Using Oxide-Etched Silicon Nanowire Biosensors. *Biosens. Bioelectron.* **2008**, *23*, 1701–1707.
20. Li, Z.; Chen, Y.; Li, X.; Kamins, T. I.; Nauka, K.; Williams, R. S. Sequence-Specific Label-Free DNA Sensors Based on Silicon Nanowires. *Nano Lett.* **2004**, *4*, 245–247.
21. Hahm, J.-I.; Lieber, C. M. Direct Ultrasensitive Electrical Detection of DNA and DNA Sequence Variations Using Nanowire Nanosensors. *Nano Lett.* **2004**, *4*, 51–54.
22. Stern, E.; Vacic, A.; Reed, M. A. Semiconducting Nanowire Field-Effect Transistor Biomolecular Sensors. *IEEE Trans. Electron Devices* **2008**, *55*, 3119–3130.
23. Zheng, G.; Patolsky, F.; Cui, Y.; Wang, W. U.; Lieber, C. M. Multiplexed Electrical Detection of Cancer Markers with Nanowire Sensor Arrays. *Nat. Biotechnol.* **2005**, *23*, 1294–1301.
24. Kim, A.; Ah, C. S.; Yu, H. Y.; Yang, J.-H.; Baek, I.-B.; Ahn, C.-G.; Park, C.-W.; Jun, M. S.; Lee, S. Ultrasensitive, Label-Free, and Real-Time Immunodetection Using Silicon Field-Effect Transistors. *Appl. Phys. Lett.* **2007**, *91*, 103901.
25. Li, C.; Curreli, M.; Lin, H.; Lei, B.; Ishikawa, F.; Datar, R.; Cote, R. J.; Thompson, M. E.; Zhou, C. Complementary Detection of Prostate-Specific Antigen Using In_2O_3 Nanowires and Carbon Nanotubes. *J. Am. Chem. Soc.* **2005**, *127*, 12 484–12 485.
26. Wang, W. U.; Chen, C.; Lin, K.-H.; Fang, Y.; Lieber, C. M. Label-Free Detection of Small-Molecule−Protein Interactions by Using Nanowire Nanosensors. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 3208–3212.
27. Zhang, G.-J.; Zhang, L.; Huang, M. J.; Luo, Z. H. H.; Tay, G. K. I.; Lim, E.-J. A.; Kang, T. G.; Chen, Y. Silicon Nanowire Biosensor for Highly Sensitive and Rapid Detection of Dengue Virus. *Sens. Actuators, B* **2010**, *146*, 138–144.
28. Chiang, P.-L.; Chou, T.-C.; Wu, T.-H.; Li, C.-C.; Liao, C.-D.; Lin, J.-Y.; Tsai, M.-H.; Tsai, C.-C.; Sun, C.-J.; Wang, C.-H.; et al. Nanowire Transistor-Based Ultrasensitive Virus Detection with Reversible Surface Functionalization. *Chem.—Asian J.* **2012**, *7*, 2073–2079.
29. Patolsky, F.; Zheng, G.; Hayden, O.; Lakadamyali, M.; Zhuang, X.; Lieber, C. M. Electrical Detection of Single Viruses. *Proc. Natl. Acad. Sci. U.S.A.* **2004**, *101*, 14 017–14 022.
30. Bae, T.-E; Jang, H.-J; Yang, J.-H.; Cho, W.-J. High Performance of Silicon Nanowire-Based Biosensors Using a High-k Stacked Sensing Thin Film. *ACS Appl. Mater. Interfaces* **2013**, *5*, 55214–5218.
31. O'Hayre, R. P.; Cha, S.-W.; Colella, W.; Prinz, F. B. *Fuel Cell Fundamentals*; John Wiley & Sons: New York, 2006.
32. Colinge, J. P.; Colinge, C. A. *Physics of Semiconductor Devices*; Springer: Berlin, 2005.
33. Bergveld, P.; Sibbald, A. *Analytical and Biomedical Applications of Ion-Selective Field Effect Transistors*; Elsevier: Amsterdam, 1988.
34. Rajendran, K.; Samudra, G. Modelling of Transconductance-to-Current Ratio (gm/ID) Analysis on Double-Gate SOIMOSFETs. *Semicond. Sci. Technol.* **2000**, *15*, 139.
35. Bousse, L.; De Rooij, N.; Bergveld, P. Operation of Chemically Sensitive Field-Effect Sensors as a Function of the Insulator-Electrolyte Interface. *IEEE Trans. Electron Devices* **1983**, *30*, 1263–1270.
36. Wipf, M.; Stoop, R. L.; Tarasov, A.; Bedner, K.; Fu, W.; Wright, I. A.; Martin, C. J.; Constable, E. C.; Calame, M.; Schönenberger, C. Selective Sodium Sensing with Gold-Coated Silicon Nanowire Field-Effect Transistors in a Differential Setup. *ACS Nano* **2013**, *7*, 5978–5983.
37. Lucovsky, G. Transition from Thermally Grown Gate Dielectrics to Deposited Gate Dielectrics for Advanced Silicon Devices: A Classification Scheme Based on Bond Iconicity. *J. Vac. Sci. Technol., A* **2001**, *19*, 1553–1561.
38. Cho, M.; Park, J.; Park, H. B.; Hwang, C. S.; Jeong, J.; Hyun, K. S. Chemical Interaction between Atomic Layer-Deposited HfO_2 Thin Films and the Si Substrate. *Appl. Phys. Lett.* **2002**, *81*, 334.
39. Green, M. L.; Ho, M.-Y.; Busch, B.; Wilk, G. D.; Sorsch, T.; Conard, T.; Brijs, B.; Vandervorst, W.; Raisanen, P. I.; Muller, D.; et al. Nucleation and Growth of Atomic Layer Deposited HfO_2 Gate Dielectric Layers on Chemical Oxide (Si-O-H) and Thermal Oxide (SiO_2 or Si-O-N) Underlayers. *J. Appl. Phys.* **2002**, *92*, 7168.
40. De Michielis, L.; Moselund, K.; Selmi, L.; Ionescu, A. M. Corner Effect and Local Volume Inversion in SiNW FETs. *IEEE Trans. Nanotechnol.* **2011**, *10*, 810–816.
41. Tadayuki, M.; Masayosi, E. Methods of ISFET Fabrication. *Sens. Actuators* **1981**, *1*, 77–96.
42. Choi, Y.-K.; Ha, D.; Snow, E.; Bokor, J.; King, T.-J. Reliability Study of CMOS FinFETs. *IEEE Int. Electron Devices Meet.* **2003**, 7.6.1–7.6.4.
43. Choi, S.; Park, I.; Hao, Z.; Holman, H. Y. N.; Pisano, A. P. Quantitative Studies of Long-Term Stable, Top-Down Fabricated Silicon Nanowire pH Sensors. *Appl. Phys. A: Mater. Sci. Process.* **2012**, *107*, 421–428.
44. Rigante, S.; Livi, P.; Wipf, M.; Bedner, K.; Bouvet, D.; Bazigos, A.; Rusu, A.; Hierlemann, A.; Ionescu, A. M. Low Power FinFET pH-Sensor with High-Sensitivity Voltage Readout. *Proc. Eur. Solid-State Device Res. Conf.* **2013**, 10.1109/ESSDERC.2013.6818890.
45. Pittino, F.; Palestri, P.; Scarbolo, P.; Esseni, D.; Selmi, L. Models for the Use of Commercial TCAD in the Analysis of Silicon-Based Integrated Biosensors. *Solid-State Electron.* **2014**, *98*, 63–69.
46. Schöning, M. J.; Tsarouchas, D.; Beckers, L.; Schubert, J.; Zander, W.; Kordoš, P.; Lüth, H. A Highly Long-Term Stable Silicon-Based pH Sensor Fabricated by Pulsed Laser Deposition Technique. *Sens. Actuators, B* **1996**, *35*, 228–233.
47. Rigante, S.; Scarbolo, P.; Bouvet, D.; Wipf, M.; Bedner, K.; Ionescu, A. M. Technological Development of High-k Dielectric FinFETs for Liquid Environment. *Solid-State Electron.* **2014**, *98*, 81–87.
48. Buitrago, E.; Fernández-Bolaños, M.; Rigante, S.; Zilch, C. F.; Schröter, N.; Nightingale, A. M.; Ionescu, A. M. The Top-Down Fabrication of a 3D-Integrated, Fully CMOS-Compatible FET Biosensor Based on Vertically Stacked SiNWs and FinFETs. *Sens. Actuators, B* **2014**, *193*, 400–412.
49. Dean, J. A. *Lange's Handbook of Chemistry*; McGraw-Hill: New York, 1999.